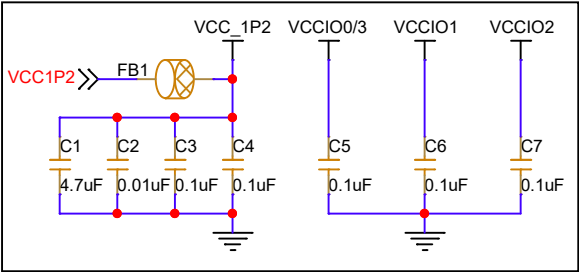
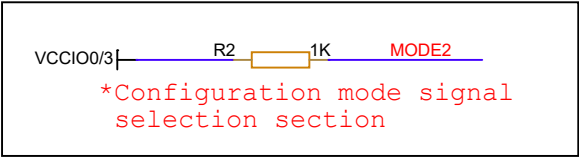
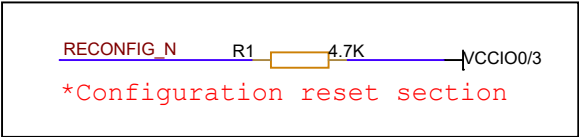
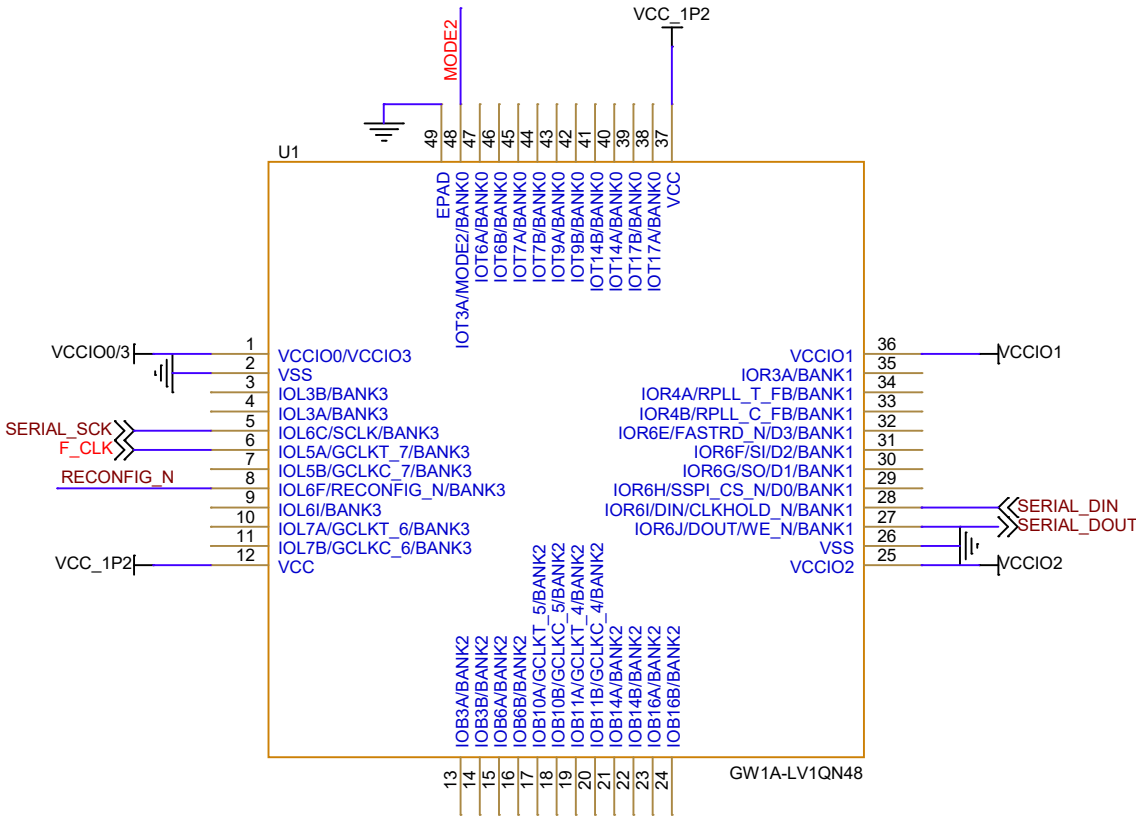


GW1A-LV1QN48



Notes:

- F_CLK signal is an external input clock signal. It is recommended that F_CLK signal be provided through an active oscillator crystal.
- It is recommended that add an ESD protection chip to the JTAG download circuit.